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1 Cache inclusion and processor sampling in multiprocessor simulations   ■
Jacqueline Chame, Michel Dubois
June 1993 **ACM SIGMETRICS Performance Evaluation Review , Proceedings of the 1993 ACM SIGMETRICS conference on Measurement and modeling of computer systems**, Volume 21 Issue 1
Full text available: ▣ pdf(1.17 MB)   Additional Information: full citation, references, citings, index terms, review

2 Using cache memory to reduce processor-memory traffic   ▬
James R. Goodman
August 1998 **25 years of the international symposia on Computer architecture (selected papers)**
Full text available: ▣ pdf(1.08 MB)   Additional Information: full citation, references, index terms

3 Modifying VM hardware to reduce address pin requirements   ▬
Matthew Farrens, Arvin Park, Gary Tyson
December 1992 **ACM SIGMICRO Newsletter , Proceedings of the 25th annual international symposium on Microarchitecture**, Volume 23 Issue 1-2
Full text available: ▣ pdf(607.69 KB)   Additional Information: full citation, references, index terms

4 Organization and performance of a two-level virtual-real cache hierarchy   ▬
W. H. Wang, J.-L. Baer, H. M. Levy
April 1989 **ACM SIGARCH Computer Architecture News , Proceedings of the 16th annual international symposium on Computer architecture**, Volume 17 Issue 3
Full text available: ▣ pdf(1.01 MB)   Additional Information: full citation, abstract, references, citings, index terms

We propose and analyze a two-level cache organization that provides high memory bandwidth. The first-level cache is accessed directly by virtual addresses. It is small, fast, and, without the burden of address translation, can easily be optimized to match the processor speed. The virtually-addressed cache is backed up by a large physically-addressed cache; this second-level cache provides a high hit ratio and greatly reduces memory traffic. We show how the second-level cache can be easily e ...

5 Eliminating the address translation bottleneck for physical address cache   ▬
Tzi-cker Chiueh, Randy H. Katz
September 1992 **ACM SIGPLAN Notices , Proceedings of the fifth international**

Web
Results **1** - **10** of about **13,600** for **data cache miss trace**. (0.79 seconds)

[PPT] Memory Spacewalking
File Format: Microsoft Powerpoint 97 - View as HTML
... benchmarks). Does **data trace** change and affect **data**/unified **cache misses**
as processor design changes ? 17. H. Distribution of dilation. ...
huron.cs.ucdavis.edu/Micro32/ presentations/p_abraham.ppt - Similar pages

CS576 Project 2: Memory Hierarchy
... Memory Reference **Trace**: The **trace** that will be provided to ... to be written directly
to L2 **data cache** and CPU ... The write-**miss** policy can be either write allocate ...
www.cs.arizona.edu/classes/ cs576/fall03/Project2/pj2.html - 9k - Cached - Similar pages

CPSC 418: Oct. 11 Lecture Notes
... 1. Instructions and **data** 2. Multiple **data** streams 3 ... Why it matters 3. How prefetching
avoids **cache** pollution III. ... separate kinds of **misses** 1. **miss**/victim **caches** ...
www.ugrad.cs.ubc.ca/spider/ cs418/2001-fall/notes/10.11.html - 6k - Cached - Similar pages

[PPT] Reducing **Cache Misses**
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... 6. Second Level **Caches**. Small **caches** have poorer **miss** rate, but.... ... separate I +
D **caches**. eg Direct Mapped (maximise tag/**data** access overlap). ... 8. **Trace Cache** (1). ...
www.cs.man.ac.uk/~watson/CS3002/lect16.ppt - Similar pages

[PDF] Microsoft PowerPoint - Lecture17.ppt
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... Algorithms? **Data** Structures ... 3 Small and simple **cache** - + 0 Avoiding address translation
+ 2 Pipeline **cache** access + 1 **Trace cache** + 3 hit time **miss** pen alt ...
clue.eng.iastate.edu/~zzhang/ courses/cpre585_f03/slides/Lecture17.pdf - Similar pages

Xeon and Events
... **misses** > not **data misses**? What do you call a μop-**miss**? NetBurst does not implement
a traditional L1 instruction **cache**. Instead it has a so-called **trace cache**. ...
www.codecomments.com/A86_Assembler/message205544.html - 19k - Cached - Similar pages

Ars Technica: P4 and G4e: an Architectural Comparison - Page 5 ...
... to kick on whenever there's an L1 **cache miss**, so it ... Since the **trace cache** functions
so differently from a normal ... will talk about the P4's L1 **data cache** and its ...
arstechnica.com/cpu/01q2/p4andg4e/p4andg4e-5.html - 31k - Cached - Similar pages

Simulating **cache** memory performance
... preparation systems like LaTeX, for example), the **data** sets for **cache** ... To determine
reasonable estimates of actual **cache miss** rates, each **cache** line should ...
web.cs.mun.ca/~paul/cs3725/ material/web/notes/node6.html - 8k - Cached - Similar pages

[PDF] Project 4 (10%): **Cache** Organization
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... **data cache** references • instruction and **data cache misses** and **miss** ... hit and a 100-cycle
miss) Output these ... 2. Address Traces An address **trace** represents the ...
www.ece.umd.edu/courses/enee350-1.F99/p4.pdf - Similar pages

Dinero IV **Trace**-Driven Uniprocessor **Cache** Simulator
... **Data** & instructions do not move in and out of ... simulation with Dinero IV is hit and
miss information. ... The various parameters of each **cache** can be set separately ...